

a controller responsive to the processor requests that creates a plurality of separate pending queues corresponding to each one of the plurality of peripheral devices for queuing the processor requests directed to a particular peripheral device in entries of a corresponding separate pending queue, wherein at least two separate peripheral devices process the processor requests simultaneously, after retrieving such processor requests from their respective separate pending queues, wherein the one or more requesting processors include dependency checking logic that generate non-blocking processor requests.

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1 41. (Once amended) The data processing system according to claim [40]
C2 39, wherein the non-blocking processor requests are generated by running real-time processes.

C3 8 (Amended)
41. [The data processing system according to claim 39 further including
]A data processing system comprising:

one or more requesting processors that generate processor requests directed to one or more peripheral devices;
a plurality of peripheral devices that accept the processor requests;
and
a controller responsive to the processor requests that creates a plurality of separate pending queues corresponding to each one of the plurality of peripheral devices for queuing the processor requests directed to a particular peripheral

device in entries of a corresponding separate pending queue, wherein at least two separate peripheral devices process the processor requests simultaneously, after retrieving such processor requests from their respective separate pending queues;

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a shared memory device, wherein the controller generates the pending queues from an allocated free pool of entries on the shared memory device, wherein the controller variably adds entries to the pending queues from the allocated free pool of entries, only after the processor requests are generated; and wherein the entries include pointers that point to memory locations on the shared memory device.

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~~51.~~ (Once amended) A data processing system comprising:

one or more requesting processors that generate non-blocking processor requests directed to one or more peripheral devices;

a plurality of peripheral devices that accept the non-blocking processor requests;

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a shared memory device; and

a memory controller responsive to the non-blocking processor requests that creates a plurality of separate pending queues on the shared memory device corresponding to each one of the plurality of peripheral devices for queuing the non-blocking processor requests directed to a particular peripheral device in entries of a corresponding separate pending queue, wherein at least two separate peripheral devices process the non-blocking processor requests simultaneously, after retrieving such non-

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blocking processor requests from their respective separate pending queues, wherein the
entries include pointers that point to memory locations on the shared memory device.

18117 (Amended)
18117 60 [The data processing system according to claim 51] A data processing system
comprising:

one or more requesting processors that generate non-blocking
processor requests directed to one or more peripheral devices;

a plurality of peripheral devices that accept the non-blocking
processor requests;

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a shared memory device; and
a memory controller responsive to the non-blocking processor
requests that creates a plurality of separate pending queues on the shared memory device
corresponding to each one of the plurality of peripheral devices for queuing the non-
blocking processor requests directed to a particular peripheral device in entries of a
corresponding separate pending queue, wherein at least two separate peripheral devices
process the non-blocking processor requests simultaneously, after retrieving such non-
blocking processor requests from their respective separate pending queues, wherein the
non-blocking processor requests include control information, addresses and data, and
wherein the shared memory device is partitioned for storing the address and control
information in a first memory array and for storing the data in a second separate memory
array.

19 61 (Once amended) A method for processing data comprising the steps of:

generating processor requests that are directed to a plurality of peripheral devices by one or more requesting processors;

creating a plurality of separate pending queues that correspond to each one of the plurality of peripheral devices, for queuing the processor requests directed to a particular peripheral device in entries of a corresponding pending queue; [and]

processing two separate processor requests directed to corresponding peripheral devices simultaneously, after retrieving such processor requests from their respective separate pending queues;

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allocating a shared memory space for entries of the separate pending queues:

freeing the entries of the processor requests in the pending queues,
after such processor requests are accepted by the peripheral devices; and

placing the outstanding processor requests in the entries of a return queue on the shared memory space, after the corresponding peripheral devices respond to such outstanding processor requests.

26 70.1 ^{25 (Amended)} [The method for processing data according to claim 61 further including] A method for processing data comprising the steps of:

generating processor requests that are directed to a plurality of peripheral devices by one or more requesting processors;

creating a plurality of separate pending queues that correspond to each one of the plurality of peripheral devices, for queuing the processor requests directed to a particular peripheral device in entries of a corresponding pending queue;

processing two separate processor requests directed to corresponding peripheral devices simultaneously, after retrieving such processor requests from their respective separate pending queues; and

freeing entries of the processor requests in the return queue, after transmitting corresponding responses from the peripheral devices to the requesting processors.

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11. (Once amended) A system for processing data comprising:
means for generating processor requests that are directed to a plurality of peripheral devices by one or more requesting processors;
means for creating a plurality of separate pending queues that correspond to each one of the plurality of peripheral devices, for queuing the processor requests directed to a particular peripheral device in entries of a corresponding pending queue; [and]

means for processing at least two separate processor requests directed to corresponding peripheral devices simultaneously, after retrieving such processor requests from their respective separate pending queues; and

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means for freeing entries of the processor requests in the return queue, after transmitting corresponding responses from the peripheral devices to the requesting processors.

34/35 28.1 (Amended)
[The system for processing data according to claim 71 further including:] A system for processing data comprising:

means for generating processor requests that are directed to a plurality of peripheral devices by one or more requesting processors;
means for creating a plurality of separate pending queues that correspond to each one of the plurality of peripheral devices, for queuing the processor requests directed to a particular peripheral device in entries of a corresponding pending queue;

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means for processing at least two separate processor requests directed to corresponding peripheral devices simultaneously, after retrieving such processor requests from their respective separate pending queues;

means for allocating a shared memory space for entries of the separate pending queues; [and]

means for freeing the entries of the processor requests in the pending queues, after such processor requests are accepted by the peripheral devices; and

means for placing the outstanding processor request in the entries of a return queue on the shared memory space, after the corresponding peripheral devices respond to such outstanding processor requests.